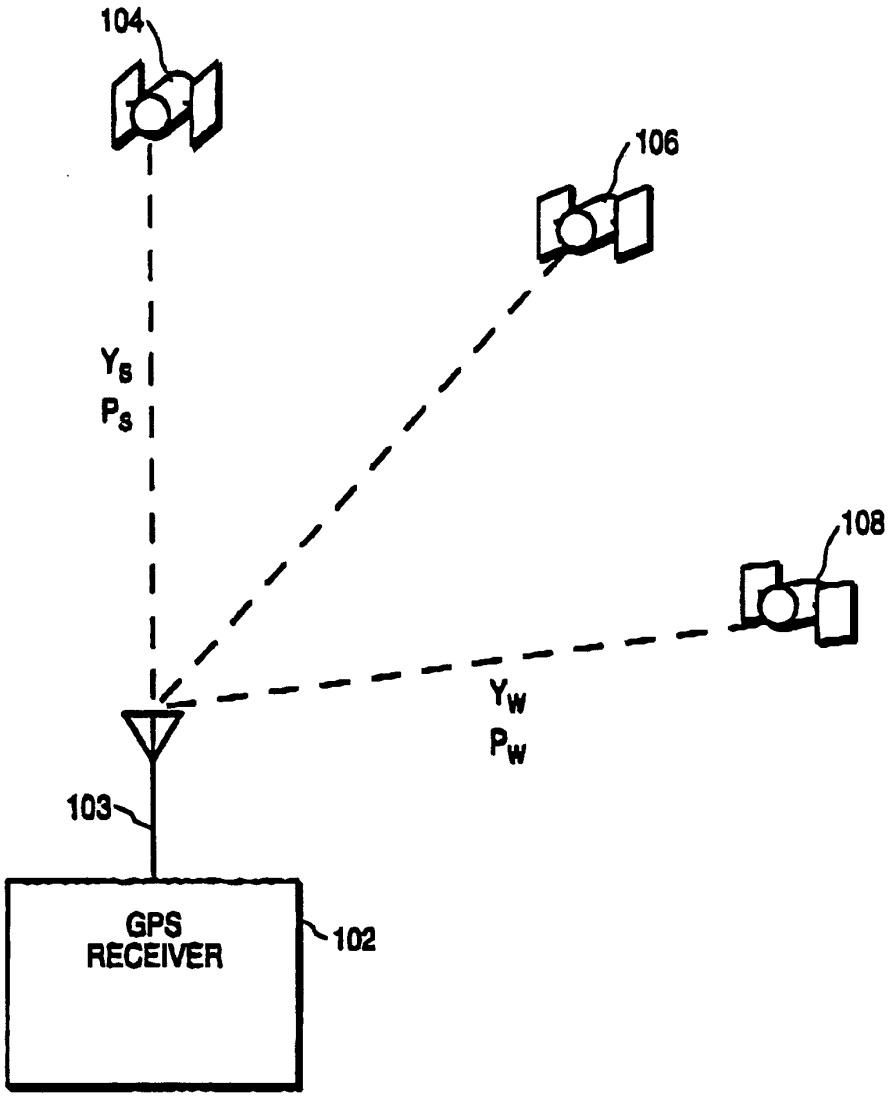

FIG.1

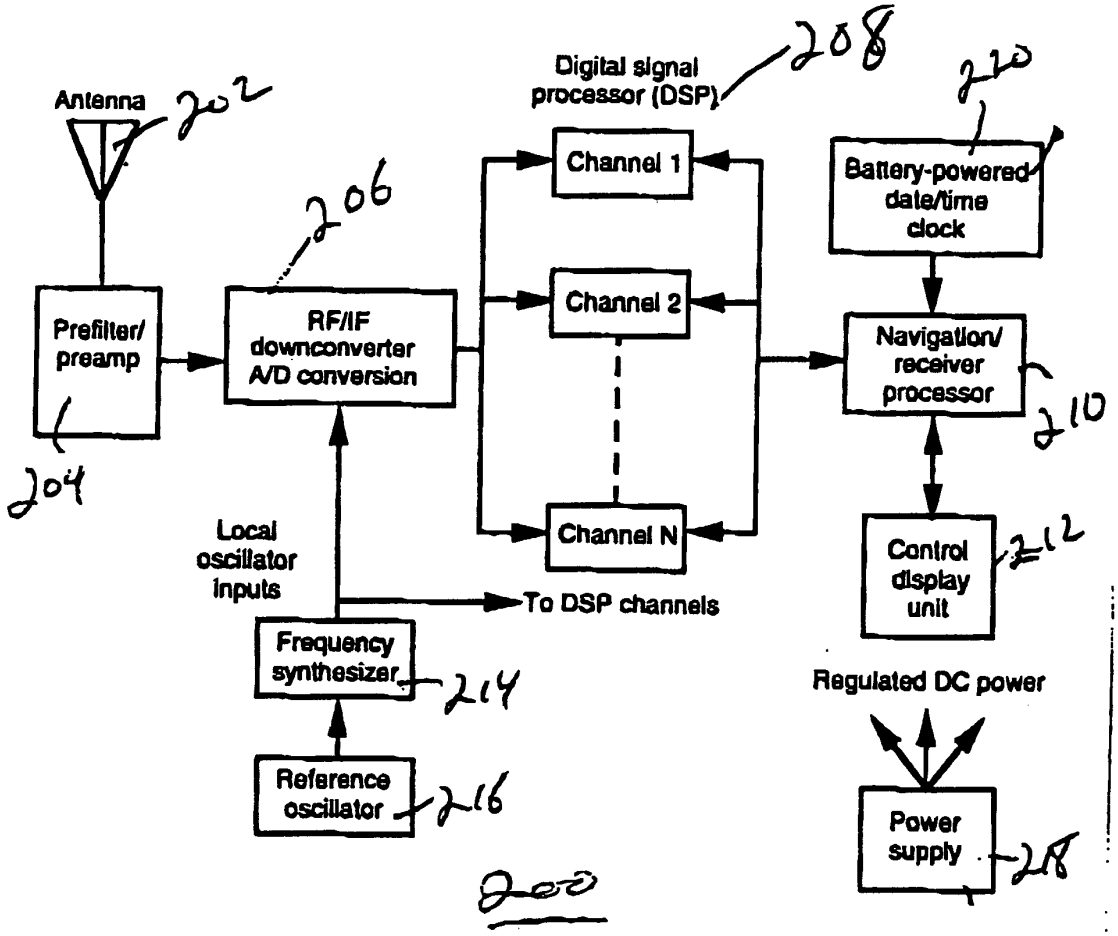
Antenna
202
Digital signal processor (DSP)
208
220
Channel 1
Battery-powered date/time clock
206
Channel 2
Prefilter/ preamp
RF/IF downconverter A/D conversion
Navigation/ receiver processor
210
204
Channel N
Local oscillator inputs
To DSP channels
Control display unit
212
Frequency synthesizer
214
Regulated DC power
Reference oscillator
216
Power supply
218
200

FIGURE 2

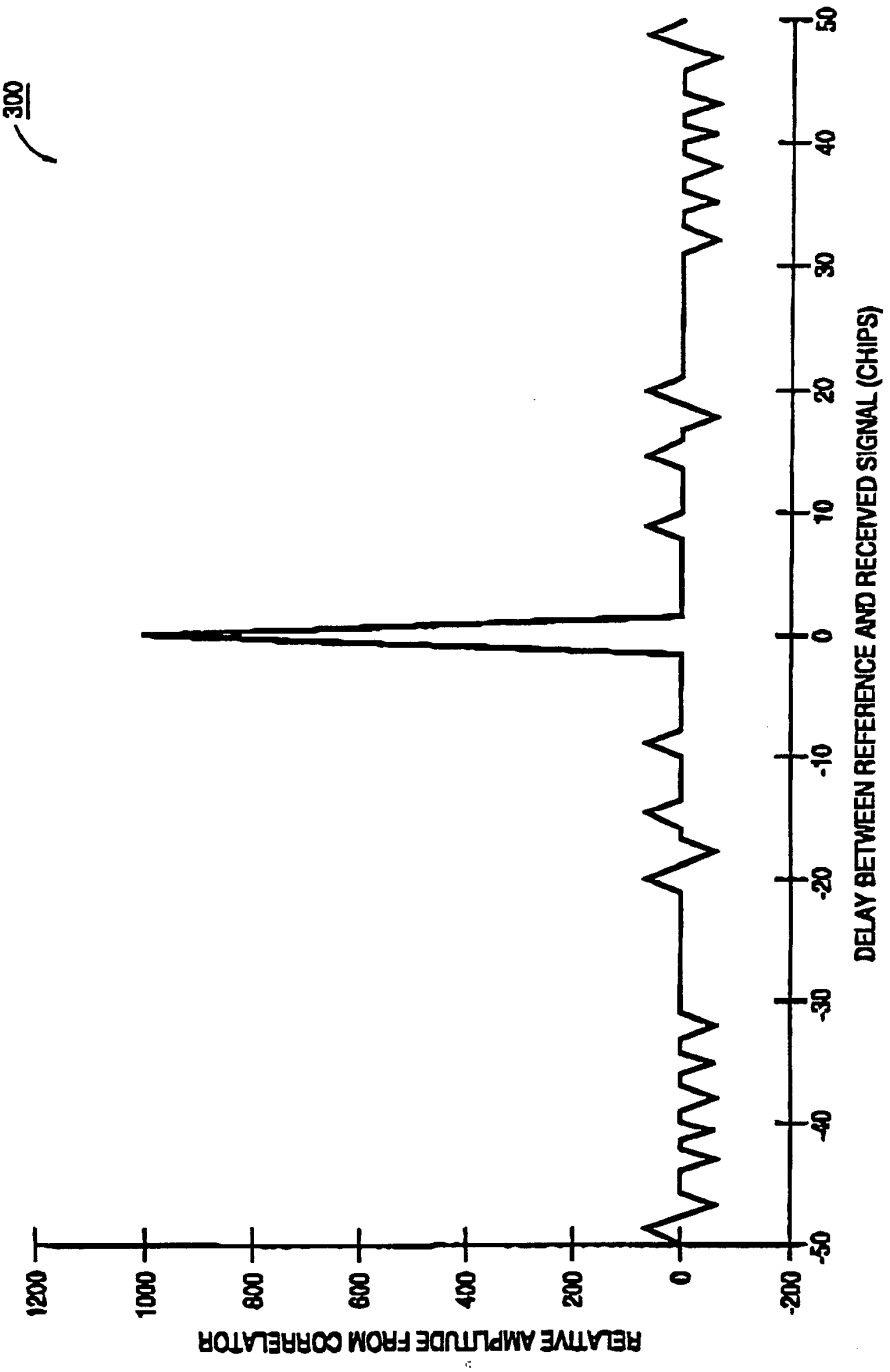
300
RELATIVE AMPLITUDE FROM CORRELATOR
1200
1000
800
600
400
200
0
-200
-50
-40
-30
-20
-10
0
10
20
30
40
50
DELAY BETWEEN REFERENCE AND RECEIVED SIGNAL (CHIPS)

FIG.3

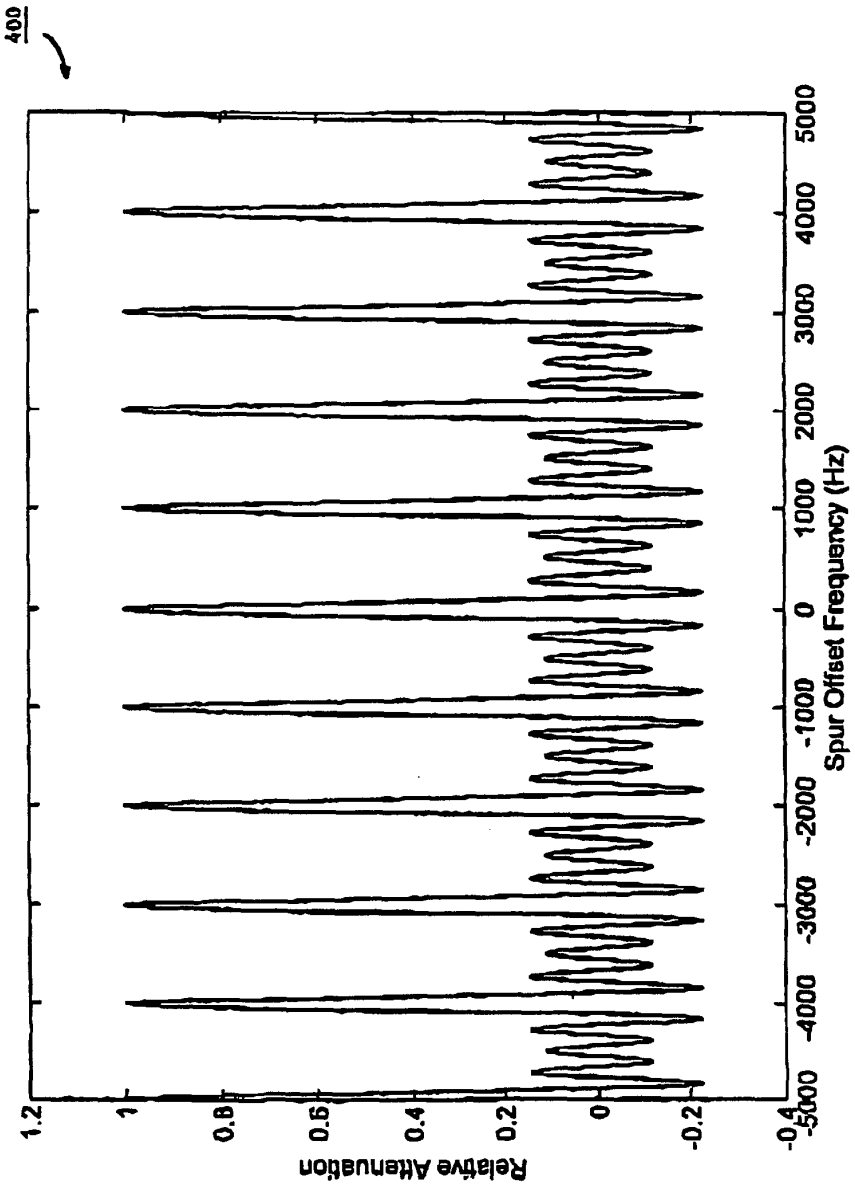
400
Relative Attenuation
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-5000
-4000
-3000
-2000
-1000
0
1000
2000
3000
4000
5000
Spur Offset Frequency (Hz)

FIG-4

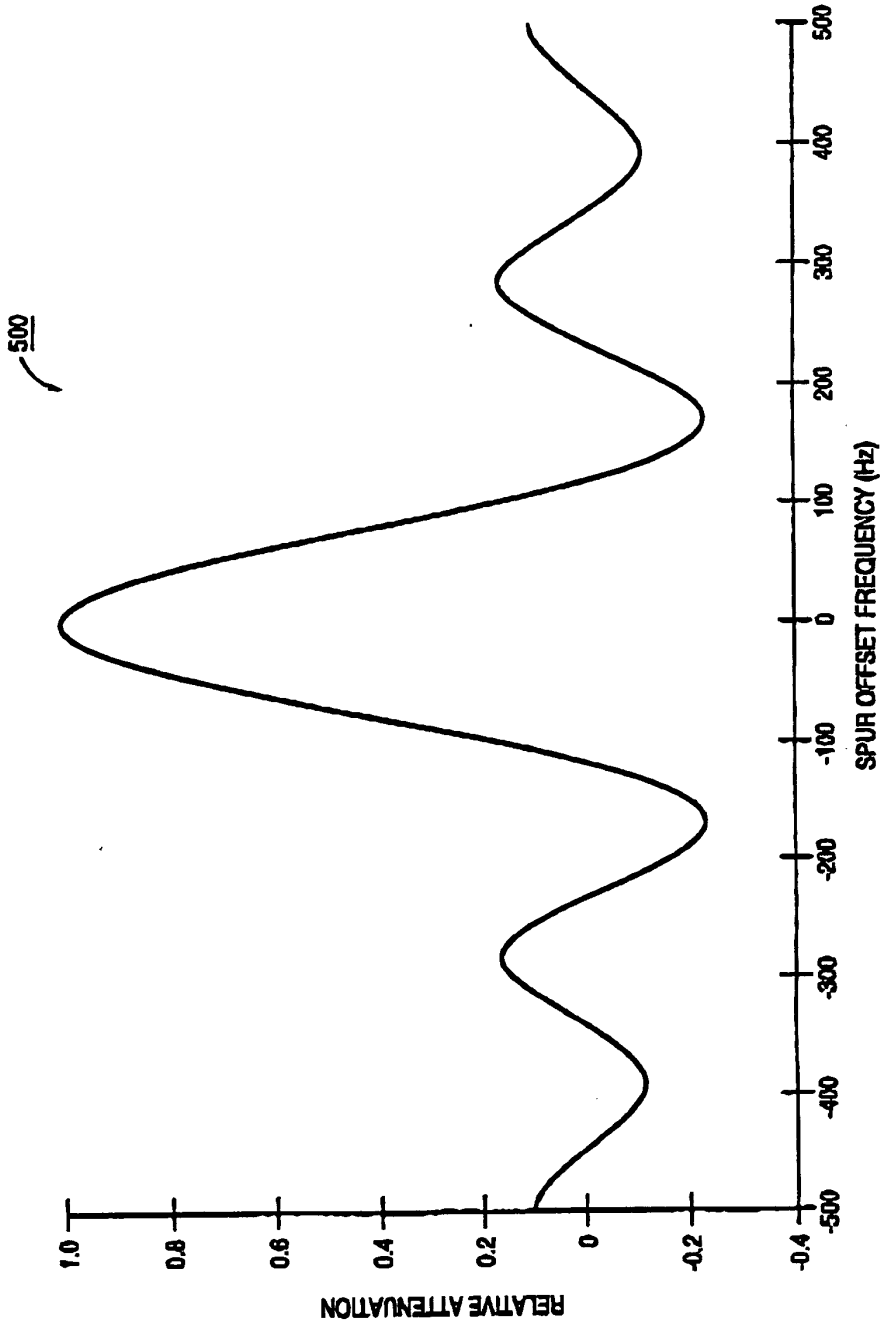
500
RELATIVE ATTENUATION
1.0
0.8
0.6
0.4
0.2
0
-0.2
-0.4
SPUR OFFSET FREQUENCY (Hz)
500
400
300
200
100
0
-100
-200
-300
-400
-500

FIG.5

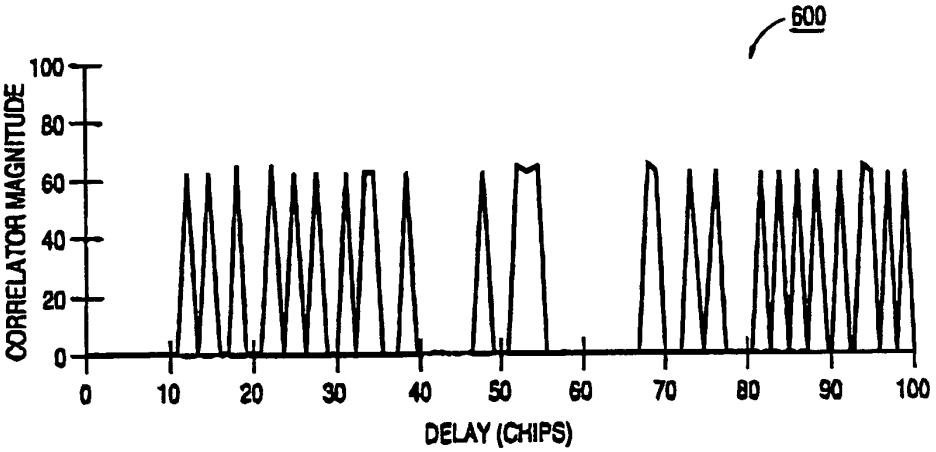
600
CORRELATOR MAGNITUDE
100
80
60
40
20
0
0
10
20
30
40
50
60
70
80
90
100
DELAY (CHIPS)

FIG.6A

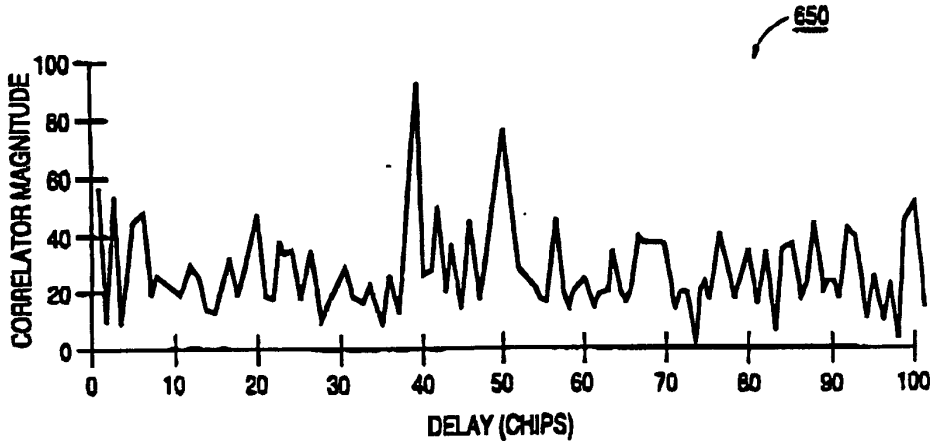
650
CORRELATOR MAGNITUDE
100
80
60
40
20
0
0
10
20
30
40
50
60
70
80
90
100
DELAY (CHIPS)

FIG.6B

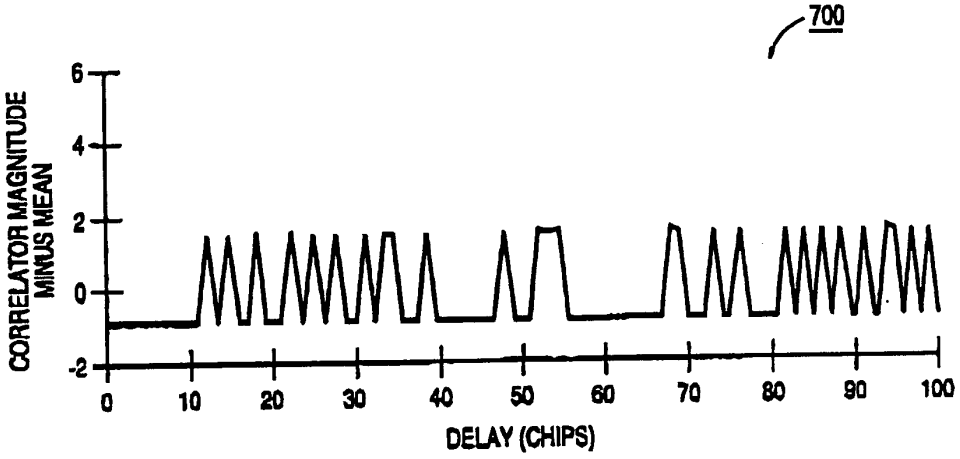
700
CORRELATOR MAGNITUDE MINUS MEAN
6
4
2
0
-2
0
10
20
30
40
50
60
70
80
90
100
DELAY (CHIPS)

FIG.7A

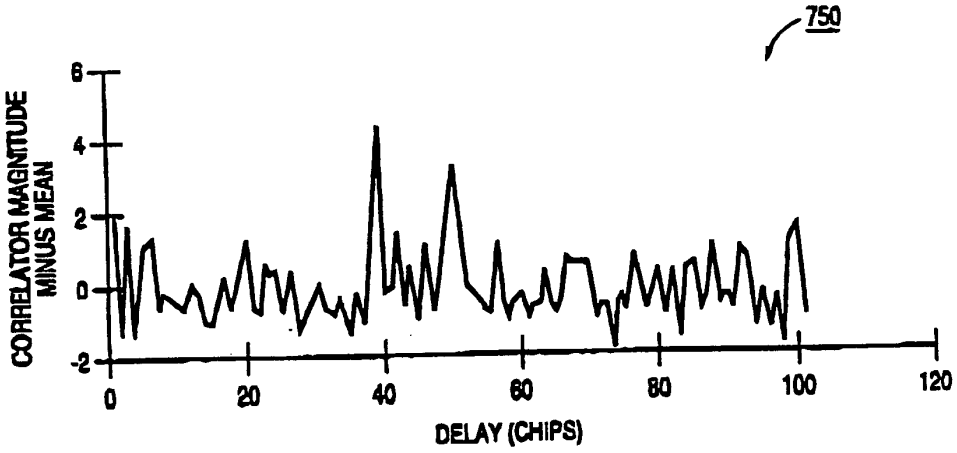
750
CORRELATOR MAGNITUDE MINUS MEAN
6
4
2
0
-2
0
20
40
60
80
100
120
DELAY (CHIPS)

FIG.7B

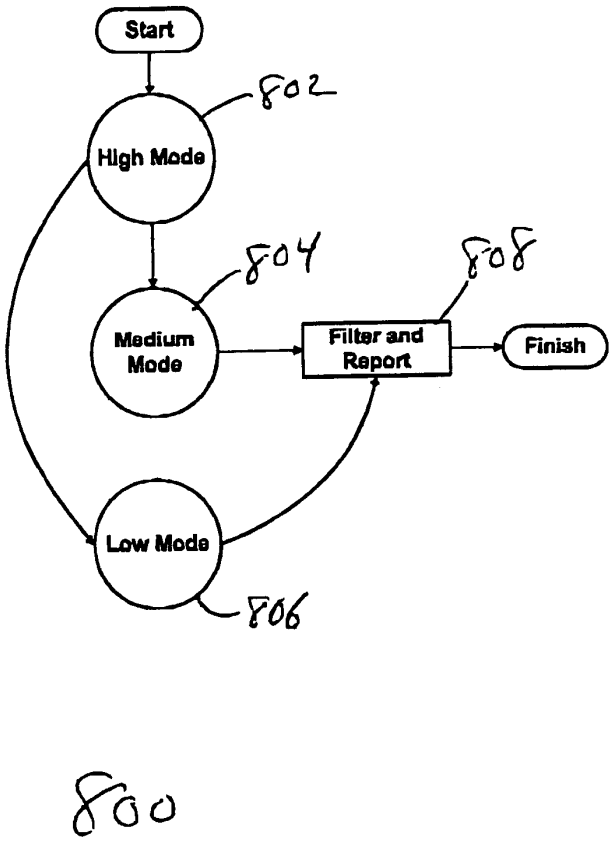

FIGURE 8a - GPS Search Mode Architecture State Machine

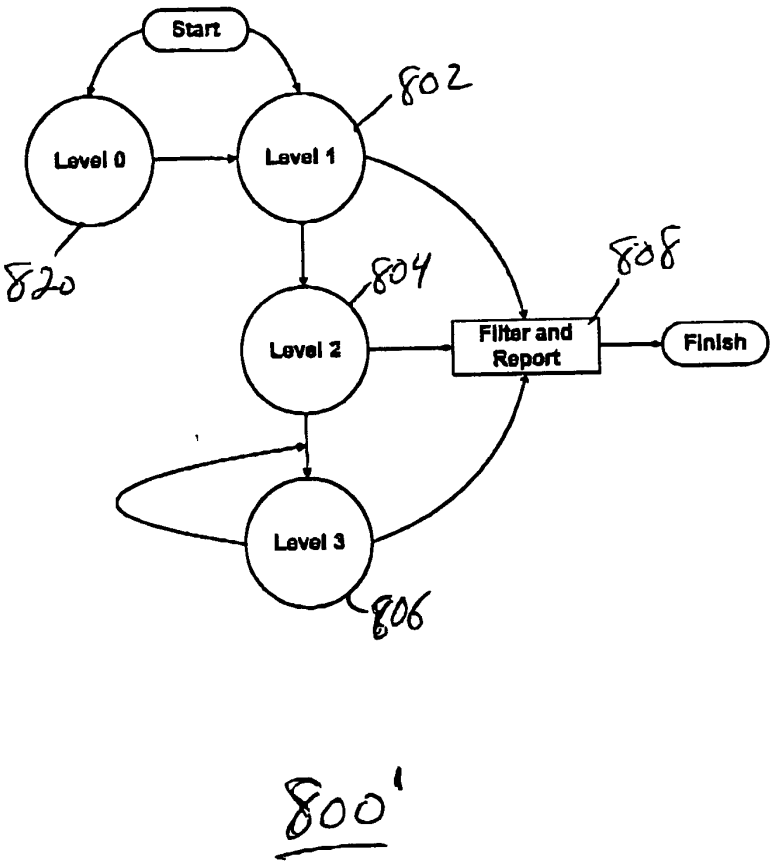

FIGURE 8b - GPS Search Mode Architecture State Machine

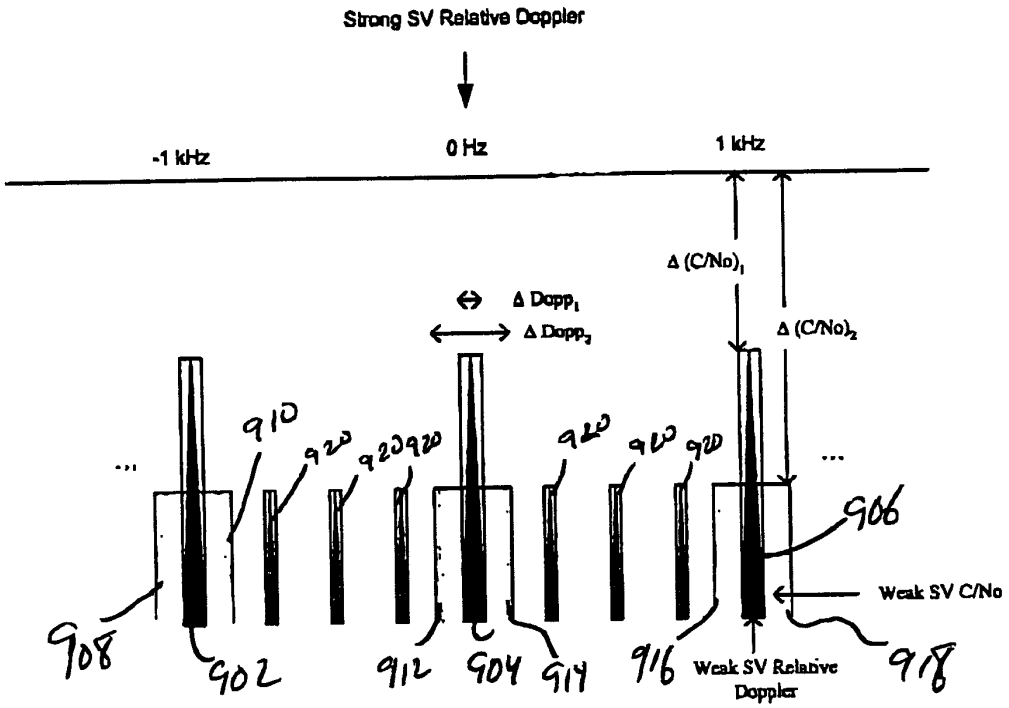

FIGURE 9 - Cross-correlation detection regions for High and Medium Search Modes

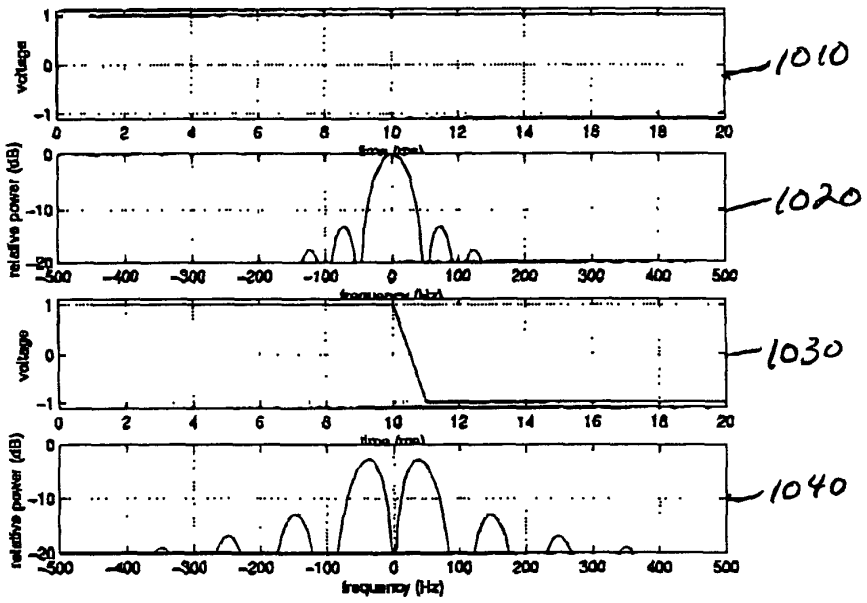

FIGURE 10 - Frequency responses of two different input sequences (20 ms coherent integration)

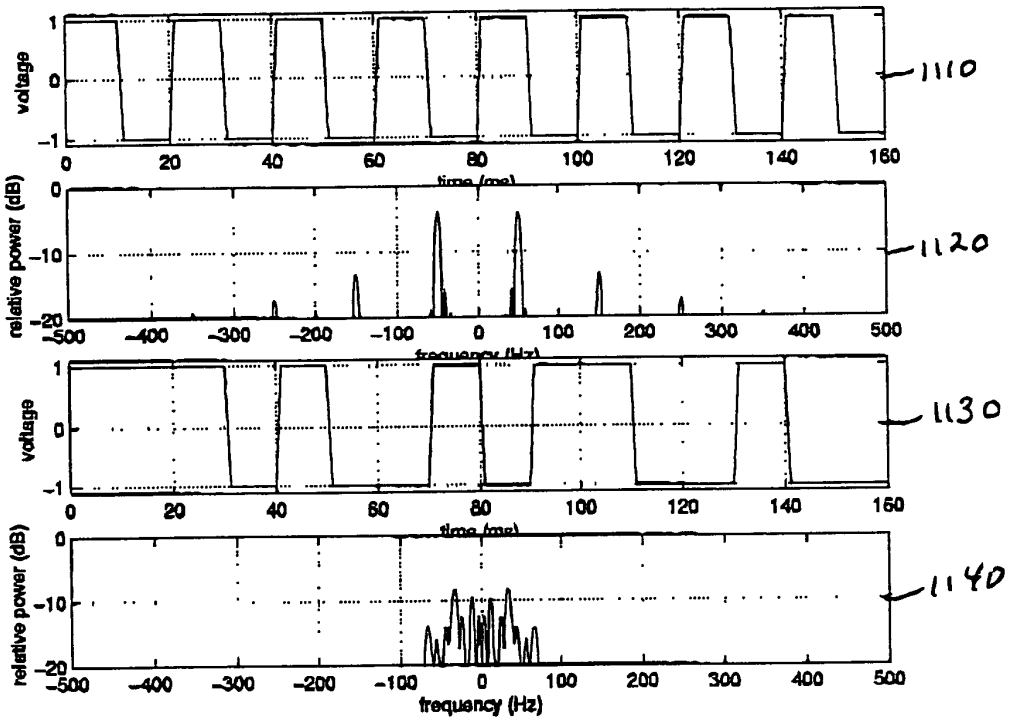

FIGURE 11 - Frequency responses of two different input sequences (160 ms coherent integration).

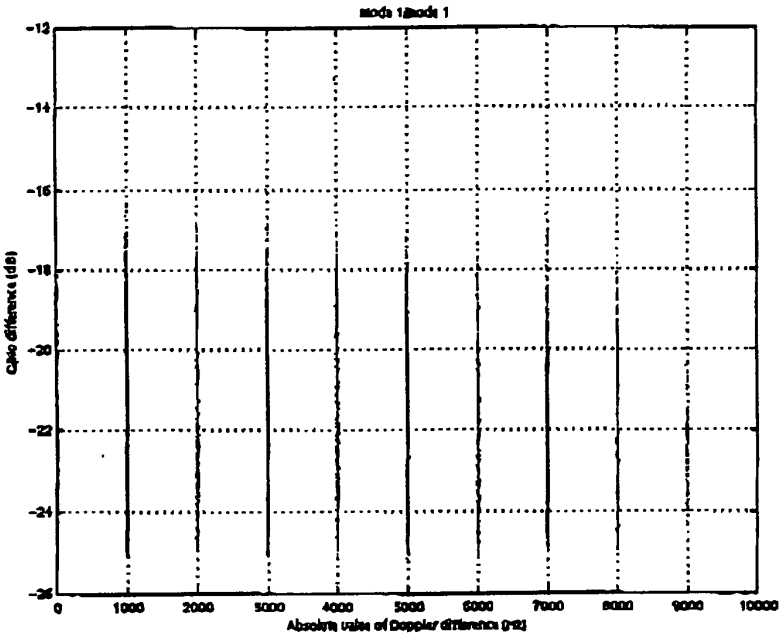
mode 1/mode 1
-12
-14
-16
-18
-20
-22
-24
-26
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000

FIGURE 12a

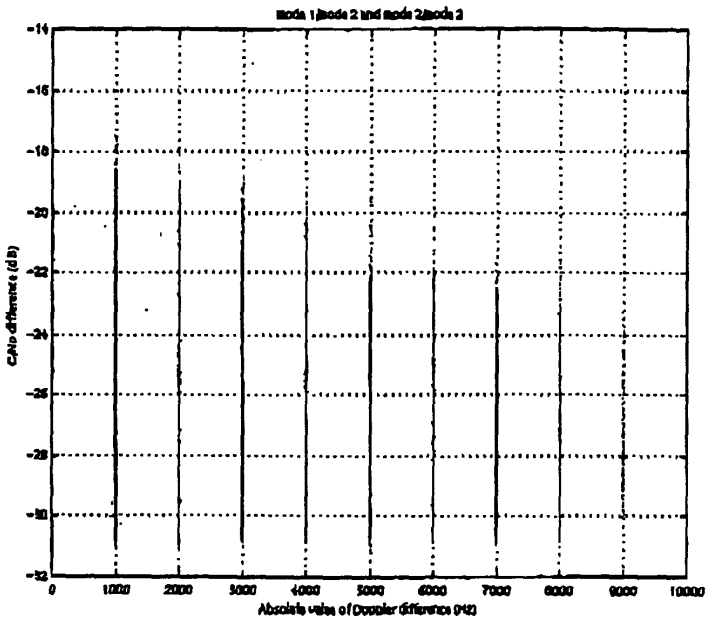
Mode 1 Mode 2 and mode 2Mode 2
-14
-16
-18
-20
-22
-24
-26
-28
-30
-32
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000

FIGURE 12b

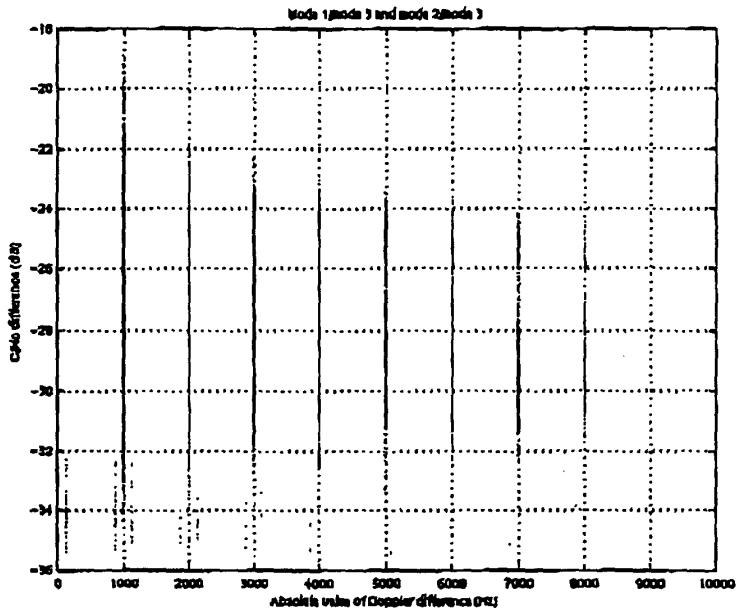
-18
-20
-22
-24
-26
-28
-30
-32
-34
-36
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000

FIGURE 12c

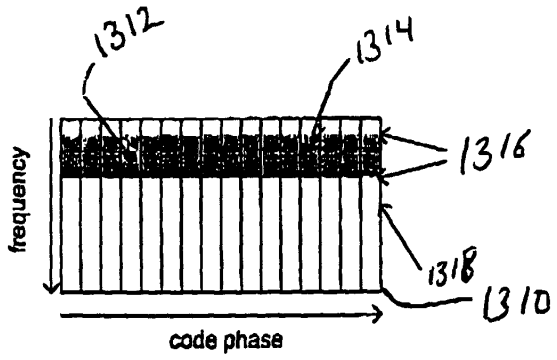

FIGURE 13a

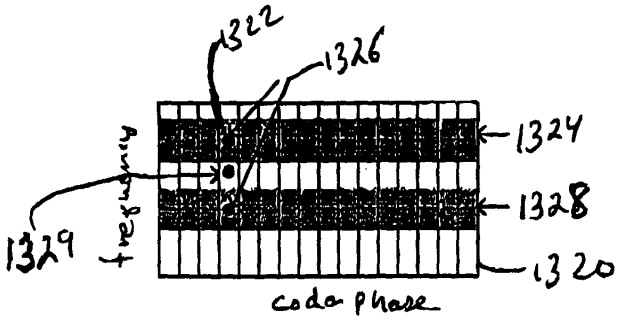

FIGURE 13b

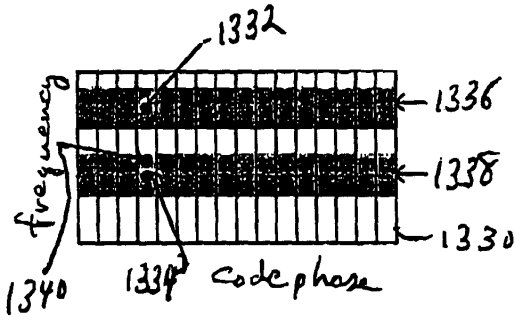

FIGURE 13c